IN THE CLAIMS:

Claim 1 (Currently Amended): A thin film transistor, comprising:

a substrate;

a crystallized semiconductor layer formed over the substrate having a channel region, low-density impurity regions and high-density impurity regions;

a gate insulating layer formed on the crystallized semiconductor layer;

a first gate electrode formed on the gate insulating layer having a width corresponding to the channel region;

a second gate electrode formed on the first gate electrode and on the gate insulating layer such that the second gate electrode overlaps the low-density impurity regions, the second gate electrode having a first portion disposed on an uppermost surface of the first gate electrode and extending substantially parallel to the substrate and second portions having substantially uniform thickness disposed along opposing sidewalls of the first gate electrode and extending substantially perpendicular to the substrate; and

a source electrode and a drain electrode respectively contacting the high-density impurity regions,

wherein a thickness of the second portions of the second gate electrode are substantially equal to a width of the low-density impurity regions and terminal ends of the second portions of the second gate electrode directly contact the gate insulating layer and are substantially parallel to the substrate.

Claim 2 (Original) The thin film transistor of claim 1, wherein the crystallized semiconductor layer is a polycrystalline silicon layer.

Claim 3 (Original) The thin film transistor of claim 1, wherein the low-density impurity regions are n$^-$ regions.

Claim 4 (Original): The thin film transistor of claim 1, wherein the high-density impurity regions are n+ regions.

Claim 5 (Original): The thin film transistor of claim 1, wherein the first gate electrode and the second gate electrode are made of the same materials.

Claim 6 (Currently Amended): The thin film transistor of claim 1, further comprising[[:]] a buffer layer formed on the substrate.

Claim 7 (Currently Amended): The thin film transistor of claim 1, further comprising[[:]] an insulating layer formed over the second gate electrode, wherein the source electrode and the drain electrode are contacted to the high-density impurity regions through respective contact holes in the insulating layer.

Claim 8 (Currently Amended): The thin film transistor of claim 1, wherein the second gate electrode layer has a substantially uniform width greater than a width of the first gate electrode layer.

Claim 9 (Original): The thin film transistor of claim 1, wherein the channel region has a width corresponding to the width of the first gate electrode layer.

Claim 10 (Currently Amended): A liquid crystal display device, comprising:

a first substrate and a second substrate;

a plurality of gate lines and data lines formed over the first substrate so as to define a plurality of pixels;

thin film transistors arranged in the plurality of pixels that each include a polycrystalline semiconductor layer including a channel region between low-density impurity regions that are in between high-density impurity regions, a gate insulating layer formed on the polycrystalline semiconductor layer, a first gate electrode formed on the gate insulating layer corresponding to the channel region, a second gate electrode formed on the first gate electrode and on the gate insulating layer such that the second gate electrode overlaps the low-density impurity regions, and a source electrode and a drain electrode contacted to the high-density impurity regions;

a pixel electrode formed in the pixel area;

a color filter layer formed on the second substrate; and

a liquid crystal layer formed between the first substrate and the second substrate,

wherein the second gate electrode has a first portion disposed on an uppermost surface of the first gate electrode and extending substantially parallel to the substrate and second portions having uniform thickness disposed along opposing sidewalls of the first gate electrode and extending substantially perpendicular to the substrate, and

wherein a thickness of the second portions of the second gate electrode are substantially equal to a width of the low-density impurity regions and terminal ends of the second portions of the second gate electrode directly contact the gate insulating layer and are substantially parallel to the substrate.

Claim 11 (Original): The liquid crystal display device of claim 10, wherein the first gate electrode and the second gate electrode are made of different materials.

Claim 12 (Currently Amended): A liquid crystal display device, comprising:

a first substrate including a pixel area and a driving circuit area;

a first thin film transistor formed in the pixel area;

a second thin film transistor formed in the driving circuit area, the second thin film transistor including ~~two~~ first and second layers of gate electrodes, a semiconductor layer having a low-density impurity regions overlapped with only one of the gate electrode layers, a source electrode and a drain electrode; and

a third thin film transistor formed in the driving circuit area,

wherein the first layer of the gate electrodes corresponds to an area between the low-density impurity regions and the second layer is disposed on the first layer and includes a first portion disposed on an uppermost surface of the first layer and extending substantially parallel to the substrate and second portions having substantially uniform thickness disposed along opposing sidewalls of the first layer and extending substantially perpendicular to the substrate, and

wherein a thickness of the second portions of the second layer are substantially equal to a width of the low-density impurity regions and terminal ends of the second portions of the second layer directly contact the gate insulating layer and are substantially parallel to the substrate.

Claim 13 (Original): The liquid crystal display device of claim 12, wherein the low-density impurity regions are n^- regions.

Claim 14 (Original): The liquid crystal display device of claim 12, wherein the third thin film transistor is a p-type thin film transistor.

Claim 15 (Withdrawn): The liquid crystal display device of claim 12, wherein the first thin film transistor is a gate overlapped lightly doped drain thin film transistor.

Claim 16 (Withdrawn): The liquid crystal display device of claim 15, wherein the first thin film transistor includes:

two layers of gate electrodes formed over the substrate;

a polycrystalline semiconductor layer arranged under the gate electrodes such that at least a part of lightly doped drain regions is overlapped by only one layer of the gate electrodes; and

a source electrode and a drain electrode.

Claim 17 (Original): The liquid crystal display device of claim 12, wherein the first thin film transistor is a lightly doped drain thin film transistor.

Claim 18 (Currently Amended): The liquid crystal display device of claim 17, wherein the first thin film transistor includes:

a polycrystalline semiconductor layer having a channel region between low-density impurity regions that are ~~in~~ disposed between high-density impurity regions;

a gate electrode arranged over the channel region; and

a source electrode and a drain electrode.

Claim 19 (Withdrawn): The liquid crystal display device of claim 12, wherein the first thin film transistor is a p-type thin film transistor.

Claim 20 (Original): The liquid crystal display device of claim 12, further comprising:

a second substrate on which a color filter layer is formed; and

a liquid crystal layer formed between the first substrate and the second substrate.

Claim 21 (Currently Amended): The thin film transistor of claim 12, wherein [[a]] the first ~~layer~~ and [[a]] second ~~layer~~ layers of the two layers of gate electrodes are made of different materials.

Claims 22-50 (Canceled).